LISTING OF THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

26. (Previously presented) A phase-locked loop (PLL) comprising:

an oscillator responsive to a control signal by producing a PLL output signal;

a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the control signal indicative of that difference, the control signal being coupled to the oscillator; and

control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency, the control circuitry including beat frequency circuitry that detects deviations of the input frequency outside the predetermined input frequency range.

27. (Previously presented) The PLL of claim 26 wherein the predetermined frequency to which the output signal is forced falls within the predetermined input frequency range.

28. (Previously presented) The PLL of claim 27 wherein the control circuit monitors the input signal's frequency and allows the PLL to lock onto the input signal should the input signal frequency return to the range of predetermined input frequencies.

29. (Previously presented) The PLL of claim 28 wherein the control circuit suppresses out of range frequency indications for a predetermined time period to allow the PLL to lock onto an input signal whose frequency has returned to within a predetermined range of input frequencies.

30. (Previously presented) A phase-locked loop (PLL) comprising:

an oscillator responsive to a control signal by producing a PLL output signal,

a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the control signal indicative of that difference, the control signal being coupled to the oscillator; and

control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency, the control circuitry including measurement circuitry which determines whether the PLL input signal's frequency deviates outside the predetermined input frequency range by measuring the voltage of said control signal coupled to the oscillator.

31. (Previously presented) The PLL of claim 30 wherein said control signal from the phase comparator is an analog signal.

32. (Previously presented) The PLL of claim 31 wherein said control signal is coupled to said oscillator through an analog to digital converter (ADC) and digital to analog converter (DAC), and the control circuit determines frequency deviations outside the predetermined input frequency range by comparing the digital signal to digital values representative of the limits of the predetermined input frequency range.

33. (Previously presented) The PLL of claim 30 wherein the predetermined frequency to which the output signal is forced falls within the predetermined input frequency range.

34. (Previously presented) The PLL of claim 33 wherein the control circuit monitors the input signal's frequency and allows the PLL to lock onto the input signal should the input signal frequency return to the range of predetermined input frequencies.

35. (Previously presented) The PLL of claim 34 wherein the control circuit suppresses out of range frequency indications for a predetermined time period to allow

the PLL to lock onto an input signal whose frequency has returned to within a predetermined range of input frequencies.

36. (Previously presented) An apparatus for providing a synchronized clock signal comprising:

a clock source that produces a clock output signal,

a PLL responsive to the clock output signal, said PLL comprising:

an oscillator responsive to a control signal by producing a PLL output signal;

a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the control signal indicative of that difference, the control signal being coupled to the oscillator; and

control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency, the control circuitry including beat frequency circuitry that detects deviations of the input frequency outside the predetermined input frequency range.

37. (Previously presented) The apparatus of claim 36 wherein the predetermined frequency to which the output signal is forced falls within the predetermined input frequency range.

38. (Previously presented) The apparatus of claim 37 wherein the control circuit monitors the input signal's frequency and allows the PLL to lock onto the input signal should the input signal frequency return to the range of predetermined input frequencies.

39. (Previously presented) The apparatus of claim 38 wherein the control circuit suppresses out of range frequency indications for a predetermined time period to allow the PLL to lock onto an input signal whose frequency has returned to within a predetermined range of input frequencies.

40. (Previously presented) An apparatus for providing a synchronized clock signal comprising:

a clock source that produces a clock output signal;

a PLL responsive to the clock output signal, said PLL comprising:

an oscillator responsive to a control signal by producing a PLL output signal;

a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the control signal indicative of that difference, the control signal being coupled to the oscillator; and

control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency, the control circuitry including measurement circuitry which determines whether the PLL input signal's frequency deviates outside the predetermined input frequency range by measuring the voltage of said control signal coupled to the oscillator.

41. (Previously presented) The apparatus of claim 40 wherein said control signal from the phase comparator is a analog signal.

42. (Previously presented) The apparatus of claim 41 wherein said control signal is coupled to said oscillator through an analog to digital converter (ADC) and a digital to analog converter (DAC), and the control circuit determines frequency deviations outside the predetermined input frequency range by comparing the digital signal to digital values representative of the limits of the predetermined input frequency range.

43. (Previously presented) The apparatus of claim 40 wherein the predetermined frequency to which the output signal is forced falls within the predetermined input frequency range.

44. (Previously presented) The apparatus of claim 43 wherein the control circuit monitors the input signal's frequency and allows the PLL to lock onto the input

signal should the input signal frequency return to the range of predetermined input frequencies.

45. (Previously presented) The apparatus of claim 44 wherein the control circuit suppresses out of range frequency indications for a predetermined time period to allow the PLL to lock onto an input signal whose frequency has returned to within a predetermined range of frequencies.

46. (Previously presented) The apparatus of claim 45 further comprising:

a plurality of clock signal inputs, and

a multiplexor responsive to control signals by routing a signal from one of the clock signal inputs to the input of the PLL.

47. (Previously presented) The apparatus of claim 46 wherein the PLL control circuitry is responsive to the detection of an out of range frequency by forcing the output signal of the PLL to a predetermined frequency by routing a signal from a different one of the clock signal inputs to the PLL input.

48. (Previously presented) A telecommunications network comprising:

a plurality of network elements at least two of which include a clock module that produces a clock output signal, and communications links connecting the network elements, the clock module of a first network element including a PLL connected to receive and to lock onto the clock output of another clock module within the network, the PLL comprising:

an oscillator responsive to a control signal by producing a PLL output signal;

a phase comparator responsive to a PLL input signal and the PLL output signal by detecting the phase difference between the two signals and producing the control signal indicative of that difference, the control signal being coupled to the oscillator; and

control circuitry responsive to deviations of the PLL input signal's frequency outside a predetermined input frequency range by forcing the frequency of the PLL output to a predetermined frequency, the control circuitry including measurement

circuitry which determines whether the PLL input signal's frequency deviates outside the predetermined input frequency range by measuring the voltage of said control signal coupled to the oscillator.

49. (Previously presented) A method of producing an output signal having a frequency that is proportional to the frequency of an input signal comprising the steps of:

(a) producing a control signal that is proportional to the phase difference between signals that are respectively proportional in frequency to the input and output signals,

(b) controlling the frequency of an output signal from an oscillator with said control signal such that the output signal from the oscillator is proportional in frequency to the input signal,

(c) detecting deviations of the input signal's frequency outside a predetermined input frequency range by measuring a beat frequency between the input and output signals, and

(d) forcing the frequency of the oscillator signal to a predetermined value when a deviation of the input signal's frequency outside a predetermined range is detected.

50. (Previously presented) The method of claim 49 further comprising the step of:

(e) allowing the frequency of the output signal to return to a value that is proportional to the phase difference between the input and output signals if the input signal frequency returns to the range of predetermined input frequencies.

51. (Previously presented) The method of claim 50 further comprising the step of:

(f) suppressing out of range frequency indications for a predetermined time period to allow the oscillator output signal to return to a frequency that is proportional to that of an input signal whose frequency has returned to a value within the range of predetermined input frequencies.

52. (Previously presented) A method of producing an output signal having a frequency that is proportional to the frequency of an input signal comprising the steps of:

(a) producing a control signal that is proportional to the phase difference between signals that are respectively proportional in frequency to the input and output signals,

(b) controlling the frequency of an output signal from an oscillator with said control signal such that the output signal from the oscillator is proportional in frequency to the input signal,

(c) detecting deviations of the input signal's frequency outside a predetermined input frequency outside a predetermined input frequency range by measuring the voltage of said control signal coupled to the oscillator, and

(d) forcing the frequency of the oscillator output signal to a predetermined value when a deviation of the input signal's frequency outside a predetermined range is detected.

53. (Previously presented) The method of claim 52 wherein step (c) comprises the steps of:

(c1) converting the control signal from and analog signal to a digital signal

(c2) comparing the digital signal to digital values representative of the limits of the predetermined input frequency range.

54. (Previously presented) The method of claim 53 further comprising the steps of:

(e) allowing the frequency of the output signal to return to a value that is proportional to the phase difference between the input and output signals if the input signal frequency returns to the range of predetermined input frequencies.

55. (Previously presented) The method of claim 54 further comprising the steps of:

(f) suppressing out of range frequency indications for a predetermined time period to allow the oscillator output signal to return to a frequency that is proportional to that of

an input signal whose frequency has returned to a value within the range of predetermined input frequencies.